Design Strategy for Barrel Shifter Using 2:1 Mux at 45 Nm And 90 Nm Technology Nodes

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Abstract: **designing a mux for low power to use it as a repetitive block in the barrel shifter will considerably reduce the simulation time. Our basic objective is to compare existing 2:1 multiplexers with proposed multiplexer design in term of power consumption, temperature sustainability, noise immunity and frequency, so that a fast and optimized barrel shifter can be designed by the help of it. A 2:1 multiplexer is a basic building block of the "switch logic". The multiplexer circuit is typically used to combine two or more digital signals onto a single line, by placing them there at different times. Technically, this is known as time-division multiplexing. Multiplexers can also be used as programmable logic devices. By specifying the logic arrangement in the input signals, a custom logic circuit can be created. The selector inputs then act as the logic inputs. This is especially useful in situations when cost is a factor and for modularity. The increasing prominence of portable systems and need to limit power consumption has led to rapid and innovative developments in low power VLSI design during recent years. The driving forces behind these developments are portable device applications requiring low power consumption and high throughput due to their small chip size with large density of components, increased complexity and high frequencies.**

Keywords: **Power Consumption and Temperature.**

I.   INTRODUCTION

Barrel shifter is an integral component of many computing systems due to its useful property that it can shift and rotate multiple bits in a single cycle . Barrel shifter is an important block of a floating point arithmetic block and used to shift the data by n bits. The design of barrel shifter is almost symmetric and can be done using repetitive combinational logic blocks. The shifter is an integral part of many digital designs .there are many application that require shift operation including CPUs ,floating point operation(like addition, subtraction, normalization),variable length coding etc.A barrel shifter needs nlog2 mux for n bit shifting and therefore designing a mux for low power to use it as a repetitive block in the barrel shifter will considerably reduce the simulation time .We designed and compare the various existing 2:1 multiplexer in term of power supply voltage versus power consumption and, temperature sustainability. All the post layout simulation have been performed at 45nm and 90nm technology on dsch 3.5 version and microwind 3.5 version EDA tool.

We assume A to be the input operand, B to be the shift/rotate amount, and Y to be the shifted/rotated result. We define A to be an n-bit value, where n is an integer power of two. Therefore is a log2 (n)-bit integer representing values from 0 to n-1.

Bit vector for A is denoted as $a7a6a5a4a3a2a1a0$ and the shift/rotate amount, B, is 3 bits.

Fig.1 logic diagram of barrel shifter

Table I

Operation	Y
3-bit shift right logical	$0\ 0\ 0\ a_7\ a_6\ a_5\ a_4\ a_3$
3-bit shift right arithmetic	$a_7\ a_7\ a_7\ a_7\ a_6\ a_5\ a_4\ a_3$
3-bit rotate right	$a_2\ a_1\ a_0\ a_7\ a_6\ a_5\ a_4\ a_3$
3-bit shift left logical	$a_4\ a_3\ a_2\ a_1\ a_0\ 0\ 0\ 0$
3-bit shift left arithmetic	$a_7\ a_3\ a_2\ a_1\ a_0\ 0\ 0\ 0$
3-bit rotate left	$a_4\ a_3\ a_2\ a_1\ a_0\ a_7\ a_6\ a_5$

2. MATERIALS AND METHODS

A B-bit shift right logical operation performs a B-bit right shift and sets the upper B bits of the result to zeros.

A B-bit shift right arithmetic operation performs a B-bit right shift and sets the upper B bits of the result to a $_{n-1}$, which corresponds to the sign bit of A.

A B-bit rotate right operation performs a B-bit right shift and sets the upper B bits of the result to the lower B bits of A.

A B-bit shift left logical operation performs a B-bit left shift and sets the lower B bits of the result to zeros.

A B-bit shift left arithmetic operation performs a B-bit left shift and sets the lower B bits of the result to zeros. The sign bit of the result is set to a $_{n-1}$.

A B-bit rotate left operation performs a B-bit left shift and sets the lower B bits of the result to the upper B bits of A.

Various 2:1 multiplexer circuits simulations are performed on 90nm and 45nm technologies with supply voltage ranging from 0.6V to 1.4V. In order to find out   the optimized design in terms of power, delay, power-delay product, the simulation have been carried out at varying supply voltages, temperatures and operating frequencies.

Existing 2:1 multiplexer:

DCVSL (Differential Cascode Voltage Swith Logic):

The Prior technique―of designing low power 2:1 Mux   Presented is Differential Cascode Voltage Swith Logic(DCVSL)circuit. Schematic of DCVSL circuit is shown in the Fig. 2. Cascode Voltage Switch Logic (CVSL) refers to a CMOS-type logic family which is designed for certain advantages. A logic function and its inverse are automatically implemented in this logic style. The pull-down network implemented by the NMOS logic tree generated complementary output. The advantage of DCVSL is in its logic density that is achieved by elimination of large PFETS from each logic function.
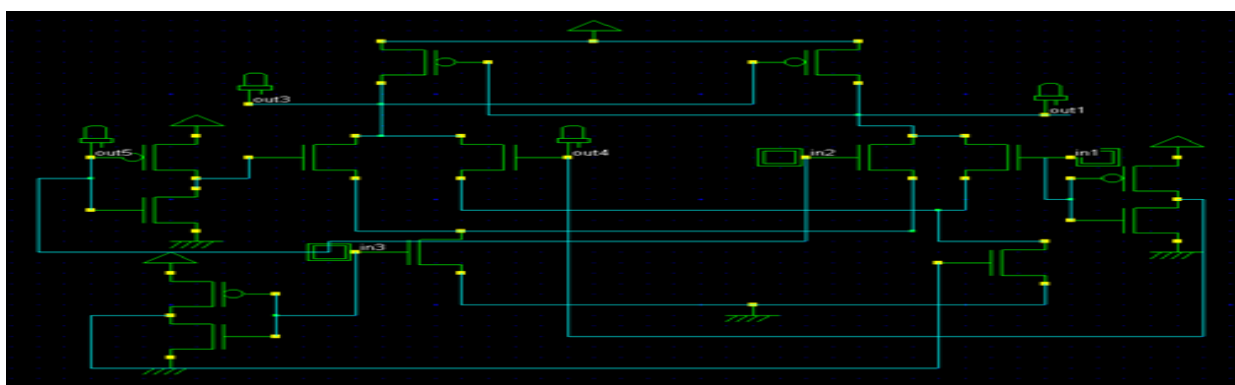

Fig. 2 Existing 2:1 Multiplexer Design (DCVSL)

Proposed 2:1 Multiplexer Design :

MDCVSL (Multiplexer double cascade voltage switch logic):

Adding two NMOS transistors T1 and T4 in the pull up part of existing 2:1 multiplexer the circuit shows a remarkable improvement over the existing design. In the proposed circuit due to the excess added transistors   there is a reduction in

threshold loss for the circuit, which further causes the reduction in overall power consumption of the circuit. Due to the transmission gate topology in the proposed design the circuit shows better output waveforms in terms of threshold loss. The two logic trees are capable of processing complex functions within a single circuit delay. The schematic of proposed design of 2:1 multiplexer in Dsch tool.
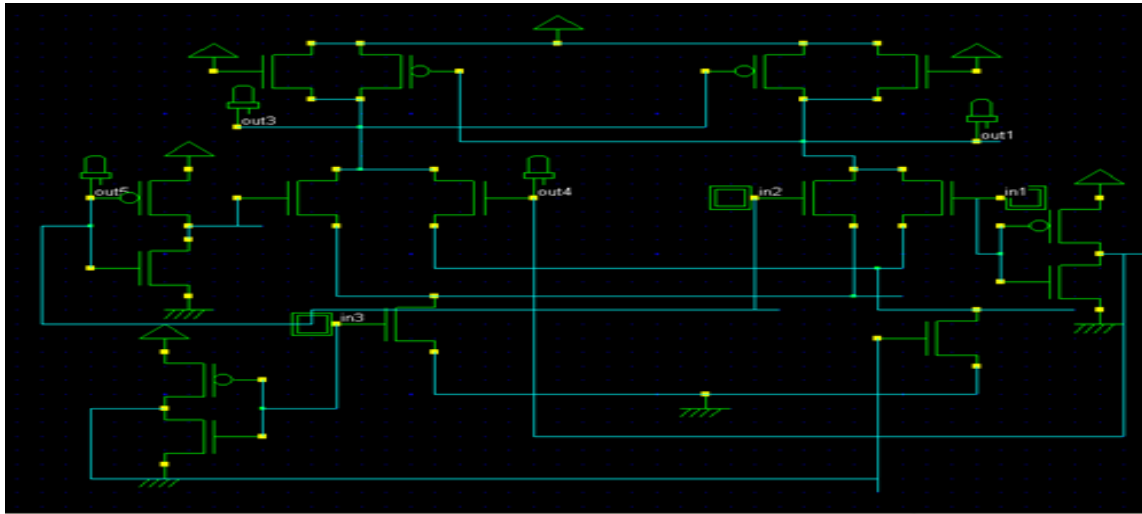

Fig. 2 proposed 2:1 Multiplexer Design (DCVSL)

3.   RESULTS AND DISCUSSION

1)   VDD versus power consumption of existing and proposed mux at 90nm and 45nm technology:

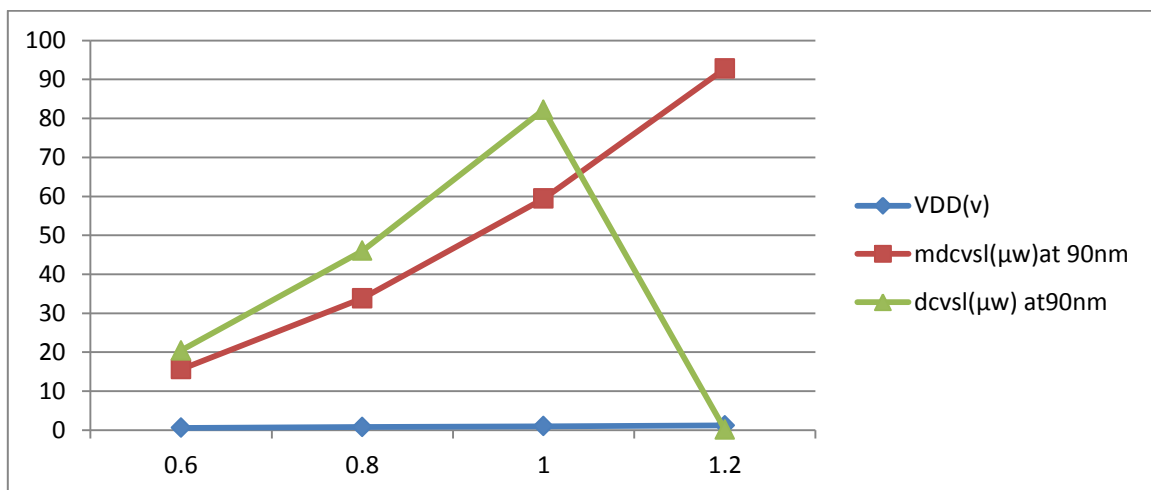| S.NO.	VDD(v)	POWER CONSUMPTION OF PROPOSED MUX(MDCVSL) 90nm (μw)	POWER CONSUMPTION Of PROPOSED MUX (MDCVSL) 45nm	POWER CONSUMPTION OF EXISTING MUX (DCVSL) 90nm	POWER CONSUMPTION OF EXISTING MUX (DCVSL) 45nm
1	0.6	15.626	7.916	20.427	9.542
2	0.8	33.836	16.653	46.004	20.253
3	1	59.422	29.276	82.201	35.462
4	1.2	92.763	46.172	0.129	55.495
5	1.4	0.134	67.730	0.186	80.622

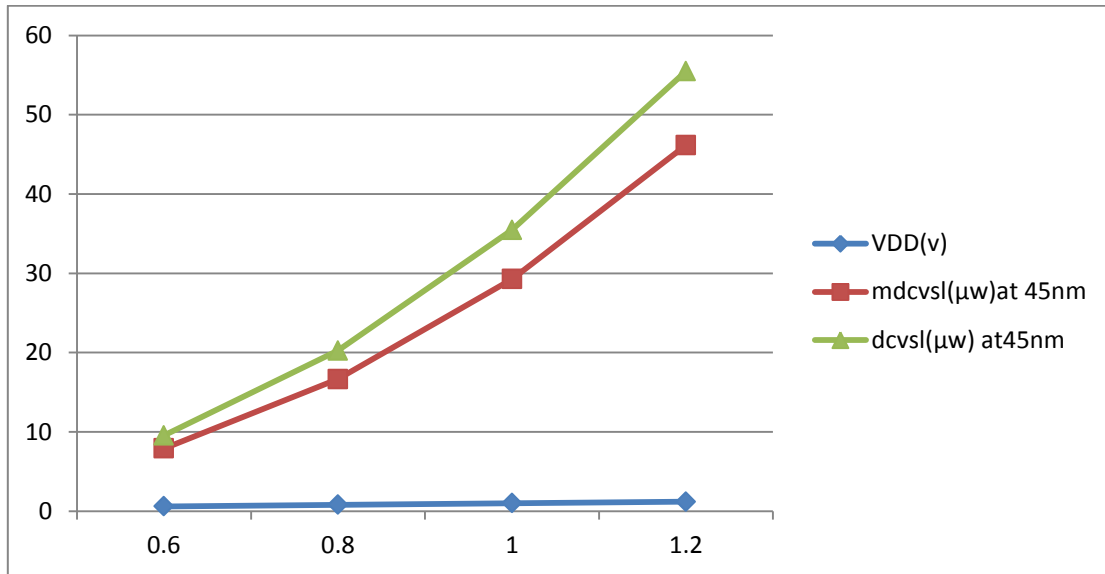**Fig.3 VDD versus power consumption at 90 nm technology**

Fig.4 VDD versus power consumption at 45 nm technology

2) **Temperature versus power consumption of existing and proposed mux at 90nm and 45nm technology:**

| S.NO.	Temp. (°C)	POWER CONSUMPTION OF PROPOSED MUX(MDCVSL) 90nm in µw	POWER CONSUMPTION Of PROPOSED MUX(MDCVSL) 45nm in µw	POWER CONSUMPTION OF EXISTING MUX (DCVSL) 90nm in µw	POWER CONSUMPTION OF EXISTING MUX (DCVSL) 45nm in µw
1	10	62.27	29.276	86.358	84.748
2	30	58.957	27.858	81.522	79.949
3	50	56.118	26.642	77.354	33.723
4	70	53.662	25.590	73.738	32.420
5	90	51.516	24.670	70.581	31.275

LAYOUT DIAGRAM OF MDVSL:
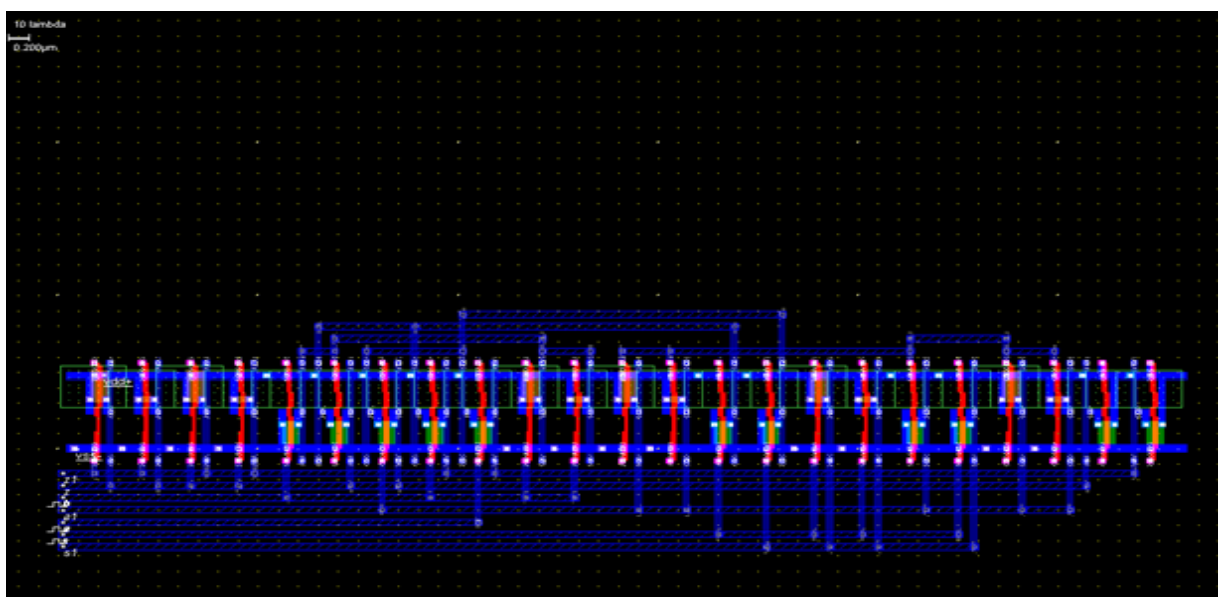
Fig.5 Layout diagram of proposed mux in 45 nm technology

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